Rationalisation of the Fibonacci Charge Pump

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***Abstract* – This paper focuses on the practical aspects of the realisation the Fibonacci charge pump (FCP). The main attention is dedicated to the study of the influence of clock frequency and the capacitance of the used capacitor to key parameters of proposed FCP. This studying is performed by measurement of four specimens of FCP with different values of capacitance and clocking frequency. The rationalisation increases the efficiency to 85 % approximately (for V_{IN} = 3 V, V_{OUT} = 34.3 V, I_{OUT} = 1 mA). The results of this work allow rational selection of capacitance in relation to requested parameters of the designed charge pump.**

Keywords-Fibonacci charge pump; rationalisation; efficiency; rise time; ripple voltage.

I. INTRODUCTION

Charge pumps are alternative to classic DC/DC converters that produce a voltage higher than supply voltage or a voltage of opposite polarity to the input. Charge pumps are used for low power applications in a range from microwatts to milliwatts, especially. These DC/DC converters fully eliminate the necessity of usage of inductors or transformers.

A standard variant of a charge pump is Dickson charge pump (DCP) [1], [2]. The Dickson charge pump is efficient and easy to integrate, but it has a relatively low voltage gain. In an ideal case, the voltage gain of each stage is the same as an amplitude of the used clock. Thus, the Dickson charge pump is useful only for a relatively low output to input voltage ratio. The no-load output voltage is calculated as [1]:

$$V_O = V_{IN} + N \cdot (V_\phi - V_D) - V_D, \qquad (1)$$

where V_O is the no-load output voltage, V_{IN} is the input voltage, N is the number of stages, V_ϕ is the amplitude of clock, V_D is the diode forward drop.

A variant of a charge pump with a higher voltage gain is a Fibonacci charge pump (FCP) [3], [4]. A principal schematic diagram of the FCP is shown in Fig. 1.

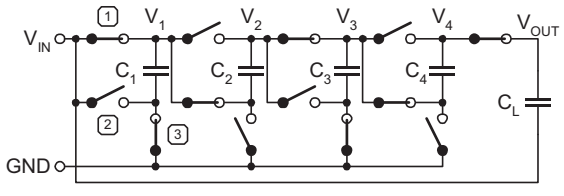

Figure 1. Principal schematic diagram of the 4-stage FCP.

The voltage gain of the FCP is gradually increased over pump stages. The voltage gain of the stage is defined as a Fibonacci number (the Fibonacci sequence is: 1, 1, 2, 3, 5, 8, …). Thus, the 4-stage FCP produces the no-load output voltage $8 \cdot V_{IN}$. Generally, the no-load output voltage of the FCP is:

$$V_O = V_{IN} + V_{IN} \cdot \sum_{n=1}^{N} F_n, \qquad (2)$$

where V_O is the no-load output voltage, V_{IN} is the input voltage, N is the number of stages, F_n is the Fibonacci number of the nth order ($F_1 = 1$, $F_2 = 1$, for $n \geq 3$: $F_n = F_{n-1} + F_{n-2}$).

The FCP circuit is more complex than a Dickson charge pump circuit solution. Furthermore, the FCP circuit has a higher sensitivity for on-chip parasitic than Dickson charge pump circuit solution. Thus, the FCP concept is especially attractive to the pump realized by discrete components [4], [5], [6].

II. FIBONACCI CHARGE PUMP REALISATION

The realisation of the FCP was solved in the previous period [6], see Fig. 2. The reference design was based on these charge pump specifications:

- power supply voltage V_{IN} = 3 V,
- the minimal steady-state output voltage V_{OUT} = 30 V at the output current I_{OUT} = 1 mA,
- the maximal ripple voltage of the output V_R = 15 mV (peak-to-peak),
- the maximal rise time of the output t_R = 65 ms.

The result of the design procedure [6] leads to the identification of values of capacitance of the transfer and load capacitors and types of active elements, see Table I.

TABLE I. RESULT DEVICE PARAMETERS

Parameter	**Value or device**
Load capacitance and transfer capacitance	$C = C_L = C_T$ = 2.2 µF
Clock frequency	f = 33 kHz
NMOS transistor	2N7002 (V_{DSS} = 60 V, $V_{GS(th)}$ = 2.1 V)
PMOS transistor	BSS84 (V_{DSS} = -50 V, $V_{GS(th)}$ = -1.7 V)
Schottky diode	PMEG4010BEA (V_{RRM} = 40 V, V_D = 0.155 V)

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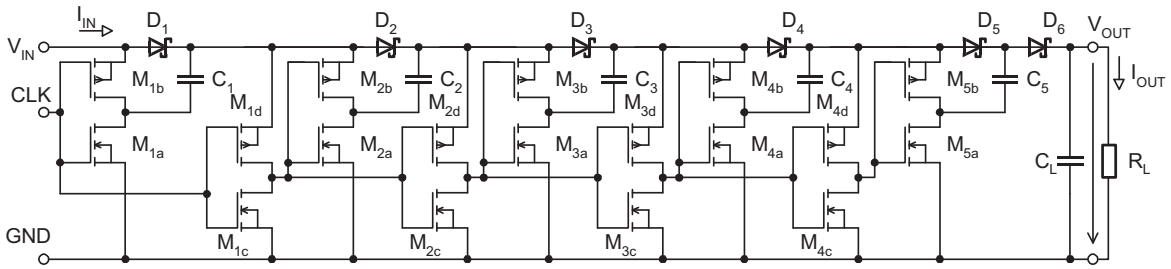

Figure 2. Schematic diagram of the 5-stage FCP.

The proposed FCP circuit solution according to Fig. 2 was successfully verified by simulation in LTspice XVII. Results from simulations confirm the functionality of this design. The output no-load voltage was V_O = 35.00 V and the output voltage at a defined load current I_{OUT} = 1 mA was V_{OUT} = 33.14 V. The rise time and the ripple voltage had values t_R = 17.37 mA and V_R = 7.24 mV (peak-to-peak) at defined load current I_{OUT} = 1 mA.

The FCP circuit solution (compare Fig. 1 and Fig. 2) is based on using transistors and diodes as switches. Switch #1 (see Fig. 1) is realised as Schottky diode D_x (x is an ordinal node number). Switch #2 (see Fig. 1) is realised as PMOS transistor M_{xb} that works as a high-side switch. Switch #3 (see Fig. 1) is realised as NMOS transistor M_{xa} that works as a low-side switch.

Auxiliary transistors M_{xc}, M_{xd} realise inverter that generates inverted and voltage shifted clock signal for the next stage of the charge pump. The presence of this inverter is essential for a regular function of the next stage and the whole charge pump. But, the auxiliary inverter implies the fact that a shoot-through current arises. Thus, the capacitor connected to the appropriate node is discharged by this shoot-through current. Therefore, the power consumption is increased, and the output voltage and the efficiency of the charge pump are decreased. This problem may be solved by a more complex circuit architecture that uses the inverter extended about an auxiliary current limiter.

The second problem of the implemented auxiliary inverter is a propagation delay. The propagation delay of inverters is gradually increased from the input to the output of the charge pump. The timing discrepancy between the stages may cause a loss of a charge. Thus, the clock frequency must be relatively low.

III. Study of Clock Frequency Influence to Parameters of the FCP

The question of enough value of the clock period is very important because strongly limits the key charge pump parameters as the efficiency and the output voltage on the one side and the secondary parameters as the rise time and ripple voltage on the other side.

The capacitance of the load capacitor C_L and the clock frequency f product marked as CFP must be a constant value for actual design because the ripple voltage [1] V_R depends on this product (4).

$$CFP = C_L \cdot f, \tag{3}$$

$$V_R = \frac{I_{OUT}}{C_L \cdot f} = \frac{I_{OUT}}{CFP}. \tag{4}$$

where I_{OUT} is the output current, other parameters are explained above.

The rise time parameter t_R is limited only by the value of capacitance C_L [2].

$$t_R = \frac{V_{OUT}}{I_{OUT}} \cdot C_L. \tag{5}$$

The study of clock frequency influence to parameters of charge pump were executed for values: C_1 = 1 µF (f_1 = 72.6 kHz), C_2 = 2.2 µF (f_2 = 33 kHz), C_3 = 4.7 µF (f_1 = 15.4 kHz) and C_4 = 10 µF (f_1 = 7.26 kHz). The CFP parameter is about 0.0726 for the values (3). Theoretically assumed results from LTspice XVII simulator is depicted on Fig. 3.

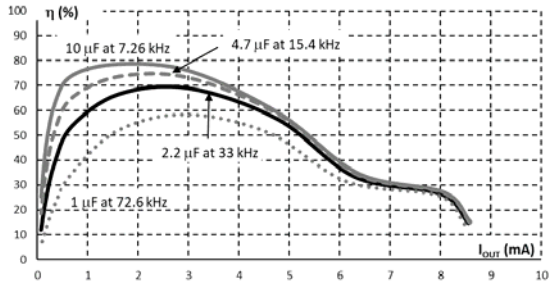

Figure 3. Efficiency vs. output current for various values of capacitance of capacitors calculated by simulation [6].

Four variants of FCP specimens with capacitances C_1 = 1 µF, C_2 = 2.2 µF, C_3 = 4.7 µF and C_4 = 10 µF were realised as double-sided PCBs, see Fig. 4.

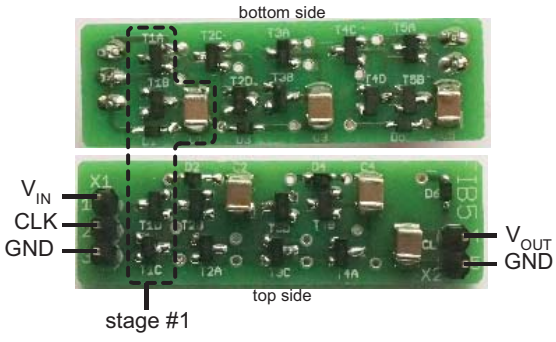

Figure 4. Photography of FCP specimen #2 (12 × 40 mm).

The key parameters of all specimens were measured by the circuit according to Fig. 5.

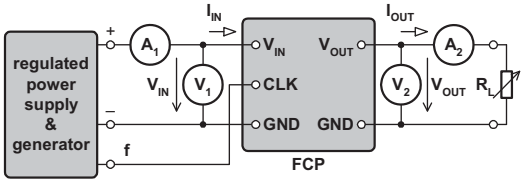

Figure 5. The circuit for V_{OUT} and η measuring.

The ammeters A_1, A_2 and voltmeters V_1, V_2 measure the input and the output currents and voltages. All ammeters measure the average value of a current [7], and the input and output voltages in the steady-state are close to DC. Thus, the calculation of the input and output power and the efficiency can be simplified to form (6) [8].

$$\eta = \frac{P_{OUT}}{P_{IN}} \cdot 100\,\% = \frac{V_{OUT} \cdot I_{OUT}}{V_{IN} \cdot I_{IN}} \cdot 100\,\%. \qquad (6)$$

The precise measurement requires that the input voltage V_{IN} has the fixed value 3 V. Thus, a voltage drop of the ammeter A_1 must be compensated by a voltage regulator. But, the clock amplitude must have the same value as the input voltage. Thus, the clock amplitude must be changed automatically with a change of the input voltage.

The measurement was simplified by a circuit according to Fig. 6. This circuit contains the regulated power source based on IC_1 (LM317T) and the frequency generator based on microcontroller IC_2 (ATtiny2313). The voltage regulator produces an input voltage for FCP that is regulated by potentiometer P. The same voltage is used for powering of the microcontroller. Thus, the microcontroller produces clock signals with the same amplitude as the regulated voltage. The microcontroller program produces two different frequencies f_1 and f_2. These frequencies are defined by the crystal resonator X and the combination of DIP switches SW according to (7).

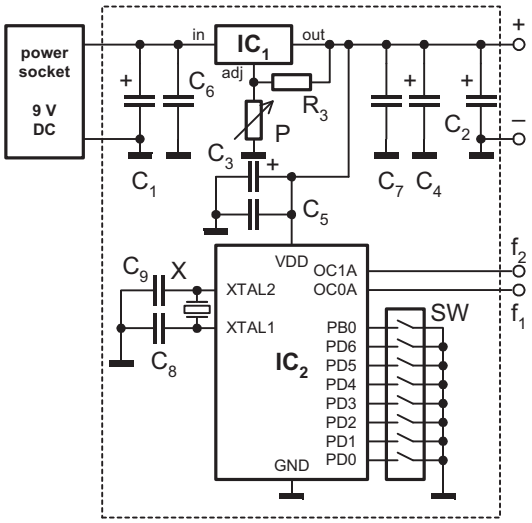

Figure 6. Schematic diagram of regulator & generator.

$$f_1 = \frac{4\,\text{MHz}}{\text{SW+1}}, \qquad f_2 = \frac{500\,\text{kHz}}{\text{SW+1}} \qquad (7)$$

where f_1, f_2 are output frequencies of the generator, *SW* is the combination of DIP switches in the range from 0 to 255.

The CFP parameter of each specimen was calculated by the formula (3). The original values C = 2.2 μF and f = 33 kHz define CFP = 0.0726. We calculate the frequency value for other values of capacitance by the same value of the CFP as:

- C = 1 μF gives f = 72.60 kHz,
- C = 4.7 μF gives f = 15.45 kHz,
- C = 10 μF gives f = 7.26 kHz.

This frequency value f_B is used as a base value for calculation other frequencies. The minimal frequency is calculated as $f_B/2$ and the maximal frequency is calculated as $2 \cdot f_B$. Last two values of frequency are calculated as $f_B/1.5$ and $1.5 \cdot f_B$. By this method, we got five values of frequency for each specimen. Practically generable value of the frequency is limited by the resolution of the microcontroller frequency generator (7). The individual values of frequency in kilo-Hertz for four specimens are:

- #1 (1 μF): 36.36, 48.20, 72.73, 108.11, 148.15,
- #2 (2.2 μF): 16.53, 22.22, 33.06, 50.00, 66.67,
- #3 (4.7 μF): 7.81, 10.42, 15.63, 23.81, 31.25,
- #4 (10 μF): 3.62, 4.85, 7.25, 10.87, 14.71.

All FCP specimen variants were measured on five values of the clock frequency according to Table II. The measured efficiency as the main parameter is documented by Fig. 7 to Fig. 10. Other results are listed in Table II.

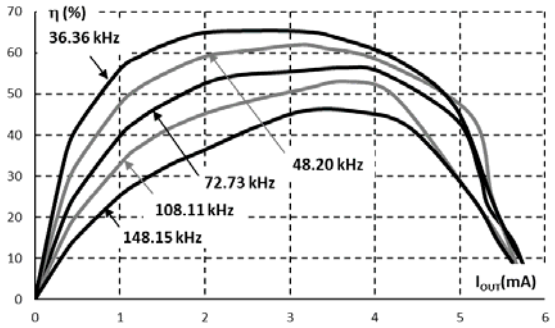

Figure 7. Efficiency vs. output current for various frequencies, variant #1: C = 1 μF.

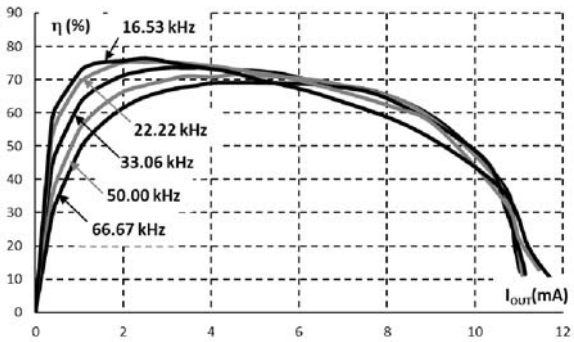

Figure 8. Efficiency vs. output current for various frequencies, variant #2: C = 2.2 μF.

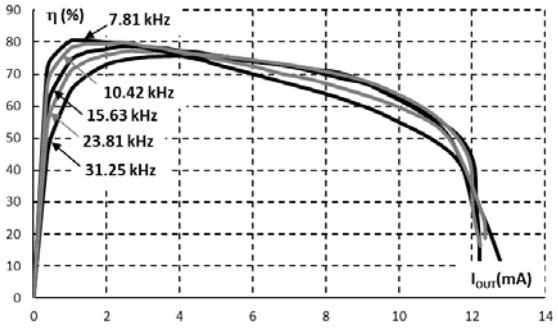

Figure 9. Efficiency vs. output current for various frequencies, variant #3: C = 4.7 µF.

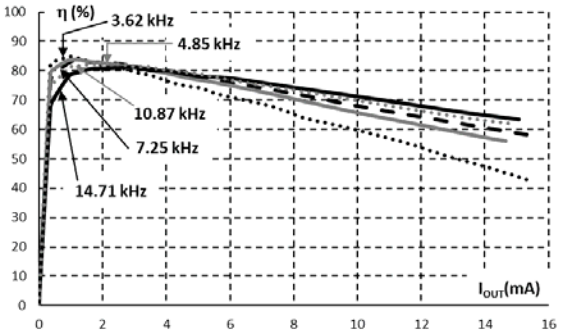

Figure 10. Efficiency vs. output current for various frequencies, variant #4: C = 10 µF.

The first variant (Fig. 7) has a strong frequency dependency, the efficiency varies in the range from 25.4 % to 56 % for the output current 1 mA. The second (Fig. 8) and the third variant (Fig. 9) are very similar. Both characteristics are flattened, thus the efficiency is close to constant value. The fourth variant (Fig. 10) is very similar to the previous two variants, too. But, in the measured range, variant #4 disposes of enough power reserve.

The rise time t_R of the output voltage was measured by the schematic diagram in Fig. 11. Firstly, the switch S was closed and after then, the input voltage and output current were set to values V_{IN} = 3 V, I_{OUT} = 1 mA in steady-state. This oscilloscope was used for measuring the ripple voltage V_R on the output. Secondly, the oscilloscope was configured for triggering by channel 1 and for a single shot and after then, the switch S was opened. The oscilloscope recorded the ramp of the output voltage after closing the switch S.

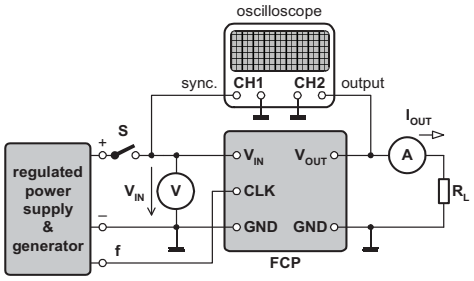

Figure 11. The circuit for t_R and V_R measuring.

The measured results of all variants for various frequencies are listed in Table II. The bold letters indicate sub-tables, the strikeout letters indicate values that miss charge pump specifications.

TABLE II. MEASURED RESULTS (V_{IN} = 3 V, I_{OUT} = 1 mA)

Variant/ parameter	**Clock frequency (kHz)**				
#1	**148.15**	**108.11**	**72.73**	**48.20**	**33.36**
V_{OUT} (V)	31.0	31.9	32.5	32.7	32.8
η (%)	25.4	34.5	39.8	47.5	56.0
t_R (ms)	18.3	18.1	17.7	17.3	16.7
V_R (mV)	5.2	5.4	6.4	10.8	26.4
#2	**66.67**	**50.00**	**33.60**	**22.22**	**16.53**
V_{OUT} (V)	33.7	33.9	34.0	34.0	33.9
η (%)	49.1	55.1	62.6	68.7	72.6
t_R (ms)	19.1	18.1	18.3	18.4	18.7
V_R (mV)	6.7	7.7	11.0	12.4	~~15.2~~
#3	**31.25**	**23.81**	**15.63**	**10.42**	**7.81**
V_{OUT} (V)	34.3	34.3	34.3	34.4	34.3
η (%)	64.0	70.6	74.4	77.8	79.9
t_R (ms)	29.6	30.4	32.0	32.2	32.6
V_R (mV)	10.2	11.4	~~18.6~~	~~26.6~~	~~37.6~~
#4	**14.71**	**10.87**	**7.25**	**4.85**	**3.62**
V_{OUT} (V)	34.5	34.4	34.4	34.5	34.3
η (%)	78.1	81.4	83.1	83.4	84.7
t_R (ms)	48.2	48.4	51.0	55.8	57.8
V_R (mV)	8.6	11.6	~~18.8~~	~~29.2~~	~~40.4~~

IV. CONCLUSIONS

Generally, the efficiency increases as the working capacitance increases and the clocking frequency decreases. Therefore, the maximal efficiency is η = 84.7 % when C = 10 µF and f = 3.62 kHz. But, the ripple voltage on output (V_R = 40.4 mV) exceeds maximal acceptable value 15 mV.

Table II gives the possibility to a rationalization of charge pump design in relation to the efficiency, rise time, ripple voltage, and capacitors cost.

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